

REMARKS

Claims 1-3, 5-14, and 16-20 are all the claims presently pending in the application. Claims 4 and 15 are canceled above. The Examiner has withdrawn claim 12 from consideration. Claims 4-8 and 15-19 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to be enabled.

It is noted that Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-3, 10-11, and 13-14 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Farooq, et al.(U.S. Patent No. 6,072,690). Claims 9 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Farooq, in view of Nagakari, et al.(U.S. Patent No. 6,573,584).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

As described and defined by, for example, claim 1, the present invention is directed to a stacked capacitor including a dielectric layer, a two-dimensional array of terminal electrodes on at least one of first and second surfaces of the dielectric layer.

First internal electrodes are stacked in multi-levels in the dielectric layer, and the first internal electrodes are electrically connected to a power line. Second internal electrodes are stacked in multi-levels in the dielectric layer, and the second internal electrodes are electrically

connected to a ground line. Vias in the dielectric layer allow the terminal electrodes to be electrically connected through the vias to the first and second internal electrodes.

The two-dimensional array further comprises at least one signal line terminal electrode such that a signal line via connected to the at least one terminal electrode is electrically isolated from the first and second internal electrodes. All of the first and second internal electrodes are spatially isolated from the low dielectric layer in the dielectric layer and each of the low dielectric layers surrounds each of the vias, thereby allowing each via to be separated from the dielectric layer.

The claimed invention, therefore, provides a stacked capacitor in which the impedance of the signal lines are reduced at high frequency because the via enclosing the signal line is surrounded by a low dielectric layer that does not contact the internal electrodes of the capacitor.

II. THE WITHDRAWAL OF CLAIM 12

The Examiner has withdrawn claim 12 from consideration. Applicants traverse this withdrawal. As pointed out in the Response to the Election/Restriction Requirement, filed September 8, 2003, it would be improper under the analysis of MPEP §806.05(c) to withdraw this claim, since it represents a combination/subcombination relationship. The claimed details are clearly shown in the combinations illustrated by Figures 10-12.

Therefore, Applicants respectfully request that the Examiner reconsider and withdraw this rejection.

III. THE 35 USC §112, FIRST PARAGRAPH REJECTION

Claims 4-8 and 15-19 stand rejected under 35 U.S.C. §112, first paragraph. The claims have been amended, above, to overcome this rejection. Specifically, independent claims 1 and 10 have been amended to clarify that there is a third type of terminal electrode, used as a signal line, that does not contact either of the two capacitor plates in the stacked capacitor.

In an exemplary embodiment shown in Figure 6, not only do the signal line terminal electrodes and vias not contact either of the two capacitor plates in the stacked capacitor, but also the low dielectric layer surrounding the signal vias also do not contact either of the two capacitor plates.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

IV. THE PRIOR ART REFERENCE

The Examiner alleges that Farooq teaches the claimed invention as described by claims 1-3, 10, 11, 13, and 14, and, when combined with Nagakari, renders obvious claims 9 and 20. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by either Farooq or Nagakari.

More specifically, in an exemplary embodiment shown in Figure 6, the signal lines that traverse the stacked capacitor of the present invention are surrounded by a low dielectric constant material different from the dielectric material encasing the capacitor plates. As clearly shown in this figure, the low dielectric constant layer 36 does not contact any of the internal electrodes 33, 34. That is, all of the first internal electrodes 33 and the second internal electrodes 34, which are connected to the power and ground lines, respectively, are separated

from the low dielectric layer 36 surrounding the via 35 connected to the third terminal electrode 32.

In contrast, Farooq discloses that the first and second internal electrodes 67,68 (e.g., reference Figure 3A) in dielectric layer 61 are in contact directly with the low dielectric layers 70, each surrounding each signal via 65 which connects pads 69 and 71 provided on opposite surfaces of the dielectric layer 61.

Therefore, in the embodiment of the present invention shown in Figure 6, the first and second internal electrodes 33,34 are separated from the low dielectric layer 36 surrounding the via 35, whereas, in Farooq, the first and second internal electrodes 67,68 are in direct contact with the low dielectric layers 70.

The above structural difference between the present invention from that of the prior art is caused by a difference in manufacturing processes. The prior art structure may be formed by a first step in which a via hole is formed in the dielectric layer 61, followed by a second step in which a low dielectric material 70 is embedded within the via hole. The third step is to form a via 65 in the low dielectric material 70.

The structure of the present invention, as shown in Figure 6, may be formed by the two following steps. First, a via hole is formed in the dielectric layer 31. Second, a via 35 is formed and a low dielectric layer 36 is formed within the via hole.

Farooq fails to teach or suggest this aspect of the present invention in which the signal via low dielectric layers are isolated from the internal electrodes.

Hence, turning to the clear language of the claims, there is no teaching or suggestion in Farooq of: "...wherein said two-dimensional array further comprises at least one signal line terminal electrode such that a signal line via connected to said at least one terminal electrode is

electrically isolated from said first and second internal electrodes, each said signal line via being surrounded by a low dielectric layer in said dielectric layer, thereby allowing each signal line via to be separated from said dielectric layer, and wherein all of said first and second internal electrodes are spatially isolated from said low dielectric layers in said dielectric layer."

The Examiner relies upon Nagakari to demonstrate the use of perovskite. However, even if Nagakari is properly combinable with Farooq, it would not overcome the deficiency identified above.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too, even in combination with Farooq or Nagakari, fails to teach or suggest the claimed invention.

V. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-3, 5-14, and 16-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

Serial No. 10/085,116
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The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 2/26/04

A handwritten signature in black ink, reading "Frederick Cooperrider". The signature is fluid and cursive, with a long horizontal line extending from the end of the name.

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